Claims

What is claimed is:

1	1.	A processor comprising:
2		A) a first register;
3		B) a means for decoding a Wait for Change instruction; and
4		C) a means for executing a Wait for Change instruction in response to
5		decoding the Wait for Change instruction, wherein:
6		execution of the Wait for Change instruction terminates when
7		either a contents of a specified location in a memory
8		differs from a contents of the first register or a specified
9		time period has elapsed.
1	2.	The processor in claim 1 wherein:
2		means (C) comprises:
3		1) a means for comparing the specified location in the memory to the
4		contents of the first register;
5		2) a means for receiving a cache invalidate signal; and
6		3) a means for waiting for the cache invalidate signal for a cache line
7		that includes the specified location in the memory when the
8		comparing in means (1) fails.
1	3.	A processor comprising:
2		A) a means for decoding a Lock instruction; and
3		B) a means for executing a Lock instruction in response to decoding
4		the Lock instruction, wherein:
5		execution of the Lock instruction terminates when either a lock
6		value is written to a specified location in a memory
7		overwriting a non-lock value in the specified location or
8		a specified time period has elapsed.

4. The processor in claim 3 wherein: 1 2 means (B) comprises: 1) a means for testing the specified location in the memory for 3 containing the non-lock value; 4 2) a means for writing the lock value to the specified location in the 5 memory when the specified location in the memory contains 6 the non-lock value; 7 3) a means for receiving a cache invalidate signal; and 8 9 4) a means for waiting for the cache invalidate signal for a cache line that includes the specified location in the memory when the 10 11 testing in means (1) fails.